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GRAYBEAL JACKSON HALEY LLP
Suite 350
155-108th Avenue N.E.
Bellevue, WA 98004-5973

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,225	PLESSIER ET AL.	
	Examiner	Art Unit	
	MARDOCHEE CHERY	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 28, 2009 has been entered.

Response to Amendment

2. In response to the last Office action, claim 1 has been canceled. Claims 2, 3, 7, 8, 9, 10, 12, 13, 14, and 15 have been amended. It is noted that the "status identifier" for claims 9 and 10 is listed as "(Original)", but should read "(Currently Amended)" to reflect the latest amendment to claims 9 and 10 filed on January 28, 2009. Claims 2-10 and 12-20 are all the claims pending.

3. The objection to the title still holds. Since none of the independent claims refer to "a bidimensional memory", the title of the invention appears to be misleading. Claim 1 referring to "a monodimensional memory" would suggest that the invention is about "monodimensional memory". To reflect the nature of using "monodimensional memory structure" to implement "a pseudo bidimensional randomly accessible memory", Applicant is encouraged to amend the title as follows: "Pseudo Bidimensional Randomly Accessible Memory using monodimensional sequentially-accessible memory structure".

4. The objections to claims 8, 14, and 15 are withdrawn in view of the amendment filed on January 28, 2009.

5. The rejection of claims 8, 12, 14, and 15 under 35 U.S.C. 112 first paragraph is withdrawn in view of the amendment filed on January 28, 2009.

Response to Arguments

6. Applicant's arguments, on pages 2-4 of the remarks, with respect to claims 8-10 and 14-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

7. Claim 8 objected to because of the following informalities:

a. Claim 8 recites "a control circuit coupled to the memory locations". However, it appears that the claim should read "a control circuit coupled to the memory", though it is understood that once the control circuit is coupled to the memory it is also coupled to the memory locations. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had

possession of the claimed invention. Particularly, claim 10 recites inter alias "...the control circuit allows sequential access to the memory locations during the write mode of operation so that the memory functions as a last-in-first-out memory...". These limitations find no support in the original disclosure as required 35 USC 112 first paragraph and consist new matter. Though the original disclosure in original claim 2 provides for "selectively feeding the first memory element with either an output of a last memory element, in the first operating configuration, or an output of a last memory element of the sub-array, in the second operating configuration", it does not provide for "allowing sequential access so that the memory functions as a last-in-first-out memory" of amended claim 8. See Waldemar Link, GmbH & Co. v. Osteonics Corp. 32 F.3d 556, 559, 31 USPQ2d 1855, 1857 (Fed. Cir. 1994); In re Rasmussen, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981). See MPEP § 2163.06 - § 2163.07(b) for a discussion of the relationship of new matter to 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 8-9 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Stone et al. (6,578,109).

As per claims 8 and 14, Stone et al. discloses a memory [Fig. 5, *cache 368*], comprising: a plurality of memory locations [Fig. 5, *cache registers 524*; col. 6, lines 47-49]; and a control circuit coupled to the memory locations [Fig. 5, *cache controller 516*; col. 6, lines 29-34] and operable to, allow random access to the memory locations during a read mode of operation [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; col. 9, lines 43-46, 58-64], and allow sequential access to the memory locations during a write mode of operation [Fig. 10, *step 1010 write request, Yes/write, step 1022 write data sequentially*; col. 10, lines 8-12].

As per claim 9 Stone discloses the control circuit allows sequential access to the memory locations during the write mode of operation so that the memory functions as a first-in-first-out [col. 10, lines 8-12].

As per claim 15, Stone et al. discloses a method, comprising: randomly accessing memory locations of a memory during either a read mode or a write mode of operation [Fig. 10, *step 1010 read/write request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data; Yes/write, step 1014 random write data to address*; col. 9, lines 43-46, 58-64], and sequentially accessing the memory locations via one of the memory locations during the read or write mode of operation [Fig. 10, *step 1030, retrieve data sequentially; step*

1022, write data sequentially; col. 10, lines 8-18], wherein the sequentially accessing occurs during the alternate mode of operation as does the randomly accessing [Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64].

As per claim 16, Stone et al. discloses wherein randomly accessing the memory locations comprises: accessing a first memory location having a first address [col. 11, lines 57-58]; and accessing a second memory location having a second address [col. 11, lines 61-62].

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone (6,578,109) and well known practice in the art.

As per claim 10 Stone discloses the control circuit allows sequential access to the memory locations during the write mode of operation so that the memory functions as a last-in-first-out [col. 10, lines 8-12]. Stone does not explicitly disclose a last-in-first-out (LIFO) memory but teaches a first-in-first-out (FIFO) memory. However, substituting

a LIFO memory for a FIFO memory is within the level of one ordinary skill in the art to substitute a LIFO memory for FIFO memory to obtain the advantage of accessing the contents of the memory in the specific order inherent to a (LIFO) memory structure.

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomaiuolo (2002/0087817) and Nojiri (4,656,625).

As per claims 8 and 14-16, Tomaiuolo discloses a memory, comprising: a plurality of memory locations [par. 006]; and a control circuit coupled to the memory locations [page 6, left column, par. 8].

Tomaiuolo does not explicitly disclose a control circuit operable to, allow random access to the memory locations during a read mode of operation, and allow sequential access to the memory locations during a write mode of operation.

Nojiri, however, discloses a control circuit operable to, allow random access to the memory locations during a read mode of operation, and allow sequential access to the memory locations during a write mode of operation [col. 12, lines 39-42; col. 13, lines 54-56].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Tomaiolo to include a control circuit operable to, allow random access to the memory locations during a read mode of operation, and allow sequential access to the memory locations during a write mode of operation because doing so would have permitted simultaneous communication

between multiple requesters (col. 1, lines 12-14) as taught by Nojiri.

15. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadanza (6,091,645), Applicant Admitted Prior Art (hereinafter APA), and Stone (6,578,109).

As per claim 3, Iadanza discloses a memory comprising: at least one array of memory elements [col. 2, ll 28-35]; a partition of the at least one array into a plurality of sub-arrays of the memory elements [Fig. 1A-1D]; an array configuration circuit for selectively putting the at least one array in one of two operating configurations, the two operating configurations including [col. 2, ll 20-27]; a sub-array selector, responsive to a first memory address, for selecting one among the plurality of sub-arrays according to the first memory address, the sub-array selector enabling access to the selected sub-array [col. 2, ll 28-36]; and a memory element access circuit, responsive to a second memory address, for enabling access to a prescribed memory element in the selected sub-array after a prescribed number of shifts, depending on the second memory address, of the data content of the memory elements in the selected sub-array, the memory blocks of each sub-array being isolated from the memory blocks of the other sub-arrays [col. 22, lines 8-18, col. 33, lines 5-10, col. 33, lines 20-24], and a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array [col. 8, ll 36-50; col. 10, ll 29-42].

Iandaza does not specifically teach a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block as required by the claim.

APA, however, discloses a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block [pars. 6 and 7] to provide a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly (pars. 6-7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Iadanza to include a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block since this would have provided a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly (pars. 6-7) as taught by APA.

Iadanza and APA do not explicitly disclose the first operating configuration is a data storage configuration, in which the memory is put when data are to be stored therein, and the second operating configuration is a data retrieval configuration, in which the memory is put when data are to be retrieved therefrom.

Stone et al., however, discloses the first operating configuration is a data storage configuration, in which the memory is put when data are to be stored therein [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; col. 9, lines 43-46, 58-64; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64], and the second operating configuration is a data retrieval configuration, in which the memory is put when data are to be retrieved therefrom [Fig. 10, *step 1010 write request, Yes/write, step 1022 write data sequentially*; col. 10, lines 8-12; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Iadanza and APA, combined, to include the first operating configuration being a data storage configuration, in which the memory is put when data are to be stored therein, and the second operating configuration being a data retrieval configuration, in which the memory is put when data are to be retrieved therefrom because doing so would have enabled implementation of effective methods

for optimizing and facilitating processor operations (col. 1, lines 60-61) as taught by Stone et al.

As per claim 2, Iadanza discloses said array configuration circuit includes, for each sub-array of memory elements, an input selector associated with a first memory element of the sub-array, for selectively feeding the first memory element with either an output of a last memory element in an adjacent previous sub-array, in the first operating configuration, or an output of a last memory element of the sub-array, in the second operating configuration [col. 2, ll 52-65; col. 5, ll 66 to col. 6, ll 12].

As per claim 3, Iadanza discloses the first operating configuration is a data storage configuration, in which the memory is put when data are to be stored therein, and the second operating configuration is a data retrieval configuration, in which the memory is put when data are to be retrieved therefrom [col. 1, ll 62 to col. 2, ll 4; col. 2, ll 28-36].

As per claim 4, Iadanza discloses in the second operating configuration each sub-array provides a respective output data, the sub-array selector selecting one sub-array output data out of the plurality of output data provided by the plurality of sub-arrays, according to the first address [col. 2, ll 28-36].

As per claim 5, Iadanza discloses said memory element access circuit enables a

transfer of the output data of the selected sub-array to a memory output after a prescribed number of shifts of the data content of the memory elements in the selected sub-array [col. 8, ll 36-50; col. 10, ll 29-42].

As per claim 6, Iadanza discloses said memory element access circuit includes a counter for counting the number of data content shifts, and a coincidence detector detecting coincidence between a counter value and a value representative of the second address, the coincidence detector enabling the transfer of the output data of the selected sub-array to the memory output when the counter value equals the value representative of the second address [col. 2, ll 36-44; col. 10, ll 10-28; col. 35, ll 34-51; col. 33, ll 25-34].

As per claim 7, Iadanza discloses each memory element includes at least one flip-flop [col. 28, ll 42-52].

16. Claims 12-13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomaiuolo (2002/0087817), Iadanza (6,091,645), and Stone et al. 6,578,109.

As per claim 12, Tomaiuolo discloses a memory, comprising: an array of memory locations [par. 005-006]; and a control circuit coupled to the array [page 6, left column, par. 8]; the memory locations comprise rings of serially coupled memory locations each

having a respective contents with the contents of each ring being independent of the contents of the other rings [page 6, left column, par. 8].

Tomaiuolo does not explicitly teach during the first mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

Iadanza, however, discloses during the first mode of operation, the control circuit is operable to control each of the rings to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59] to provide serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo and APA to include shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal since this would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

However, Tomaiuolo and Iadanza do not explicitly teach a control circuit operable to cause the array to operate as a random-access memory during a read mode of operation and a first-in-first-out memory during a write mode of operation.

Stone et al. discloses a control circuit operable to cause the array to operate as a random-access memory during a read mode of operation therein [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; col. 9, lines 43-46, 58-64; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64] and a first-in-first-out memory during a write mode of operation [Fig. 10, *step 1010 write request, Yes/write, step 1022 write data sequentially*; col. 10, lines 8-12; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: FIFO, Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Tomaiuolo and Iadanza, combined, to include a control circuit operable to cause the array to operate as a random-access memory during a read mode of operation and a first-in-first-out memory during a write mode of operation because doing so would have enabled implementation of effective methods for optimizing and facilitating processor operations (col. 1, lines 60-61) as taught by Stone et al.

As per claim 13 Tomaiuolo discloses the memory locations comprise a ring of serially coupled memory locations each having a respective contents [page 6, left column, par. 8].

However, Tomaiuolo does not specifically teach during the first mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

Iadanza discloses during the read mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59] to provide serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo and Stone et al., combined, to include shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

17. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone (6,578,109) and Iadanza (6,091,645).

As per claim 17, Stone discloses the invention as claimed with respect to claim 15. Stone further discloses reading first data from a first memory location [Fig. 10, col. 9, lines 43-46]; and reading the second data from the first memory location [col. 9, lines 45-51], but does not explicitly disclose shifting second data from a second memory location into the first memory location.

Iadanza, however, discloses shifting second data from a second memory location into the first memory location [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting second data from a second memory location into the first memory location because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 18, Stone discloses the invention as claimed with respect to claim 15. Stone further discloses writing first data to a first memory location [col. 10, lines 8-11]; writing second data to the first memory location [col. 10, lines 10-18], but does not explicitly disclose shifting the first data from the first memory location to a second memory location.

Iadanza discloses shifting the first data from the first memory location to a second memory location [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting the first data from the first memory location to a second memory location because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 19, Stone discloses the invention as claimed with respect to claim 15. Stone, however, does not explicitly disclose shifting the contents of each respective memory location to a respective next memory location a number of times; and accessing a predetermined one of the memory locations after a predetermined one of the shifts.

Iadanza discloses shifting the contents of each respective memory location to a respective next memory location a number of times [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59]; and accessing a predetermined one of the memory locations after a predetermined one of the shifts [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting the contents of each respective memory location to a respective next memory location a

number of times; and accessing a predetermined one of the memory locations after a predetermined one of the shifts because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 20, Stone discloses the invention as claimed with respect to claim 15, Stone, however, does not explicitly disclose shifting the contents of each of n respective memory locations to a respective next one of the n memory locations n times; and accessing a predetermined one of the n memory locations after a predetermined one of the n shifts.

Iadanza discloses shifting the contents of each of n respective memory locations to a respective next one of the n memory locations n times [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59]; and accessing a predetermined one of the n memory locations after a predetermined one of the n shifts [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting the contents of each of n respective memory locations to a respective next one of the n memory locations n times; and accessing a predetermined one of the n memory locations after a predetermined one of the n shifts because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

Conclusion

18. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

19. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mardochee Chery/

Examiner,

Art Unit 2188